

Test 1 – Simulation Part

Z_{load} :

To start off, my assigned f_0 was 2.6 GHz and my Q was 1.2. Using the equations on the assignment description, I designed the following circuit:

$$Q=1.2$$

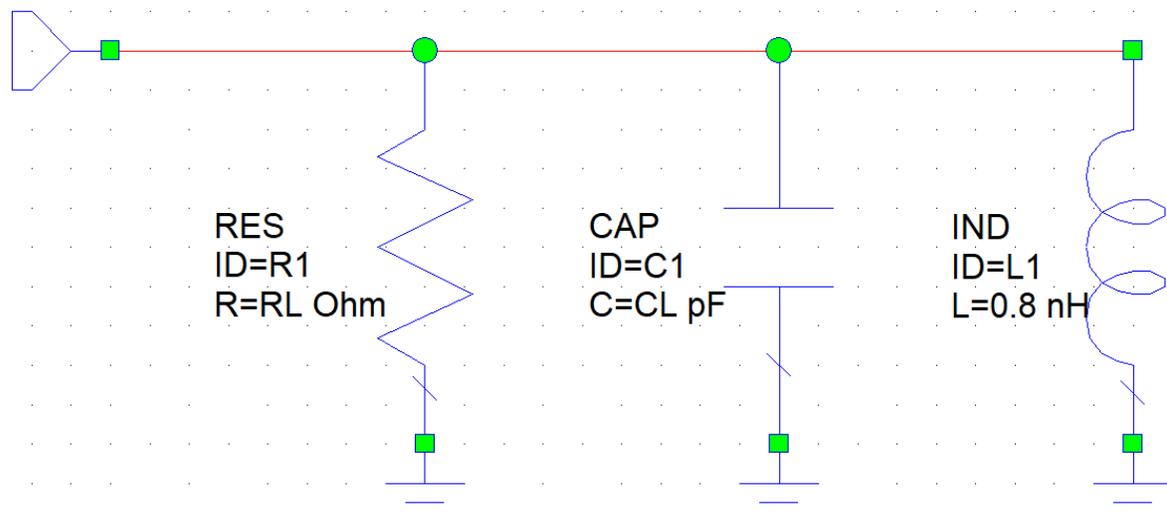
$$f_0=2.6$$

$$Q=\omega RC \quad \omega=(\text{sqrt}(LC))^{-1}$$

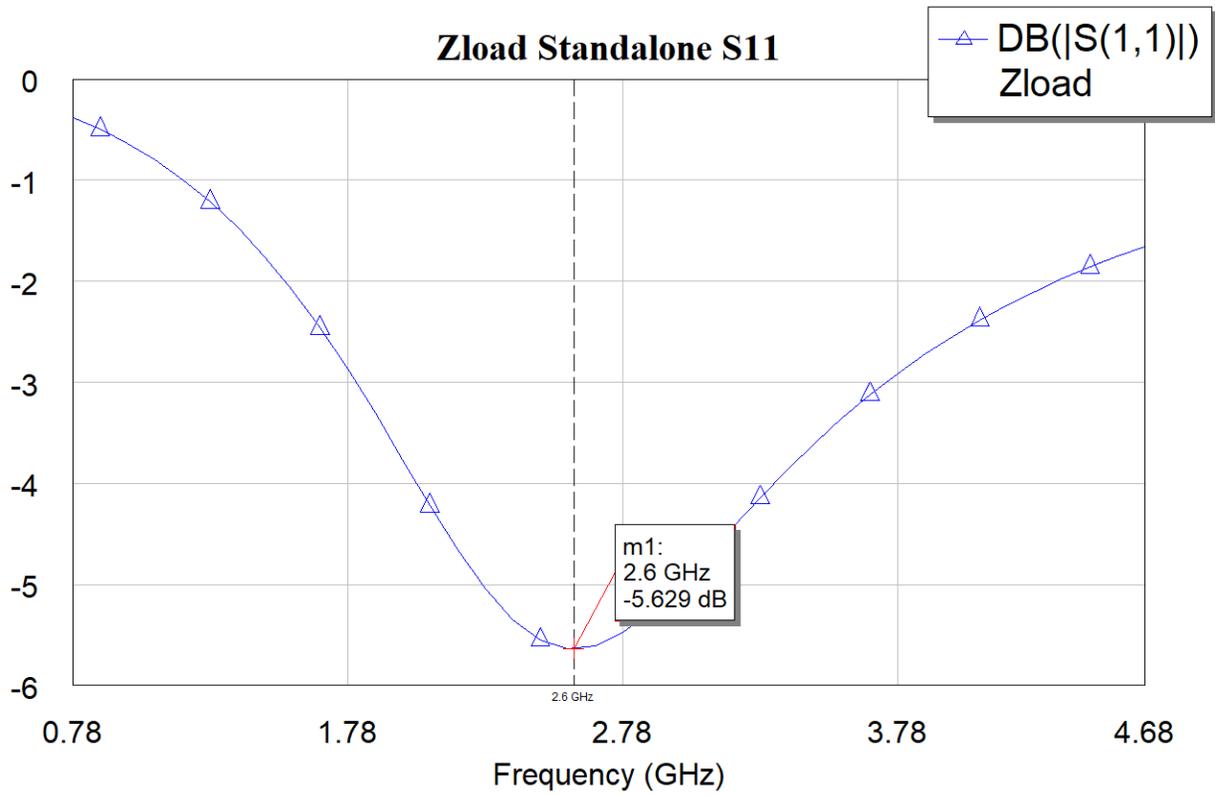
$$CL=4.68$$

$$RL=15.68$$

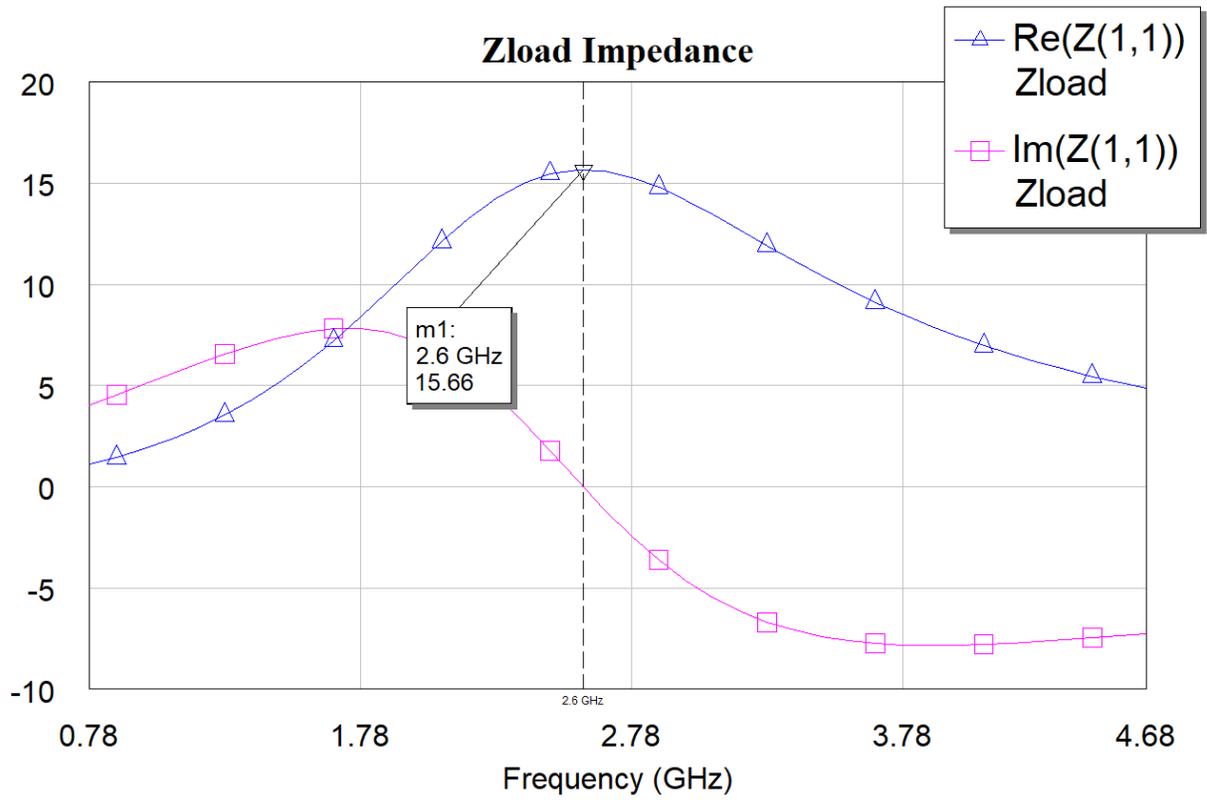
PORT
P=1
Z=50 Ohm



Which has the following reflection characteristics:

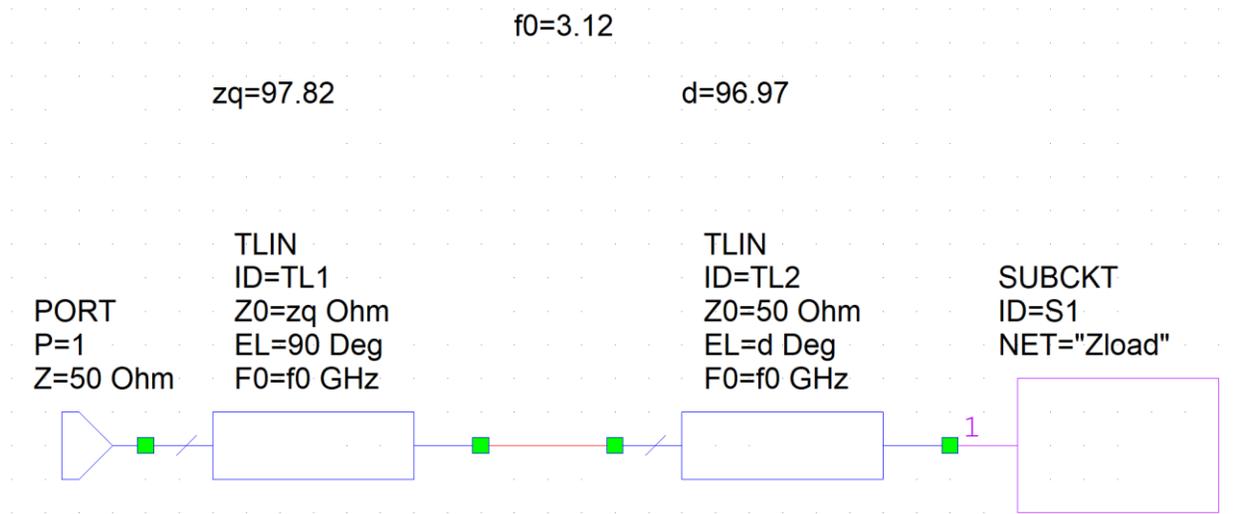


And the following impedance characteristics:

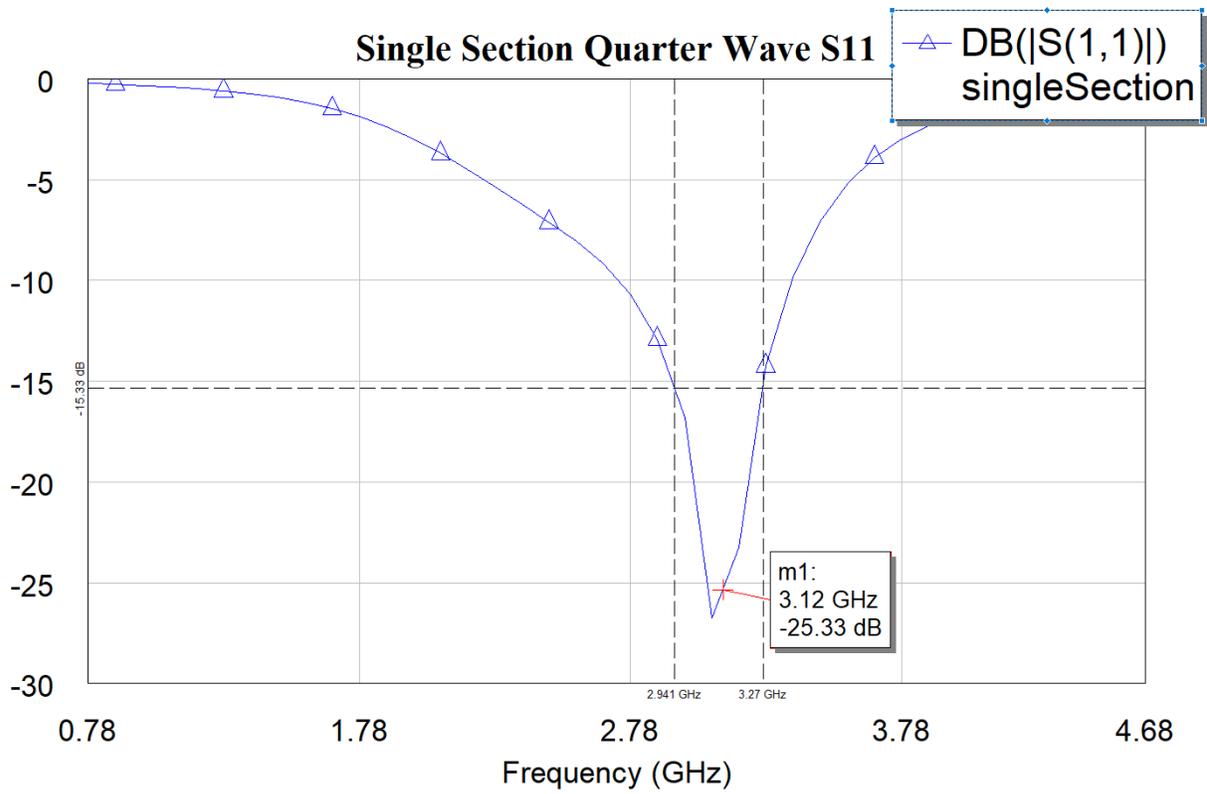


Single-section quarter-wave transformer matching circuit:

For this portion, I opted to add a transmission line between the load and the quarter-wave transformer to bring the Z'_{load} to the voltage minimum. This is the design:

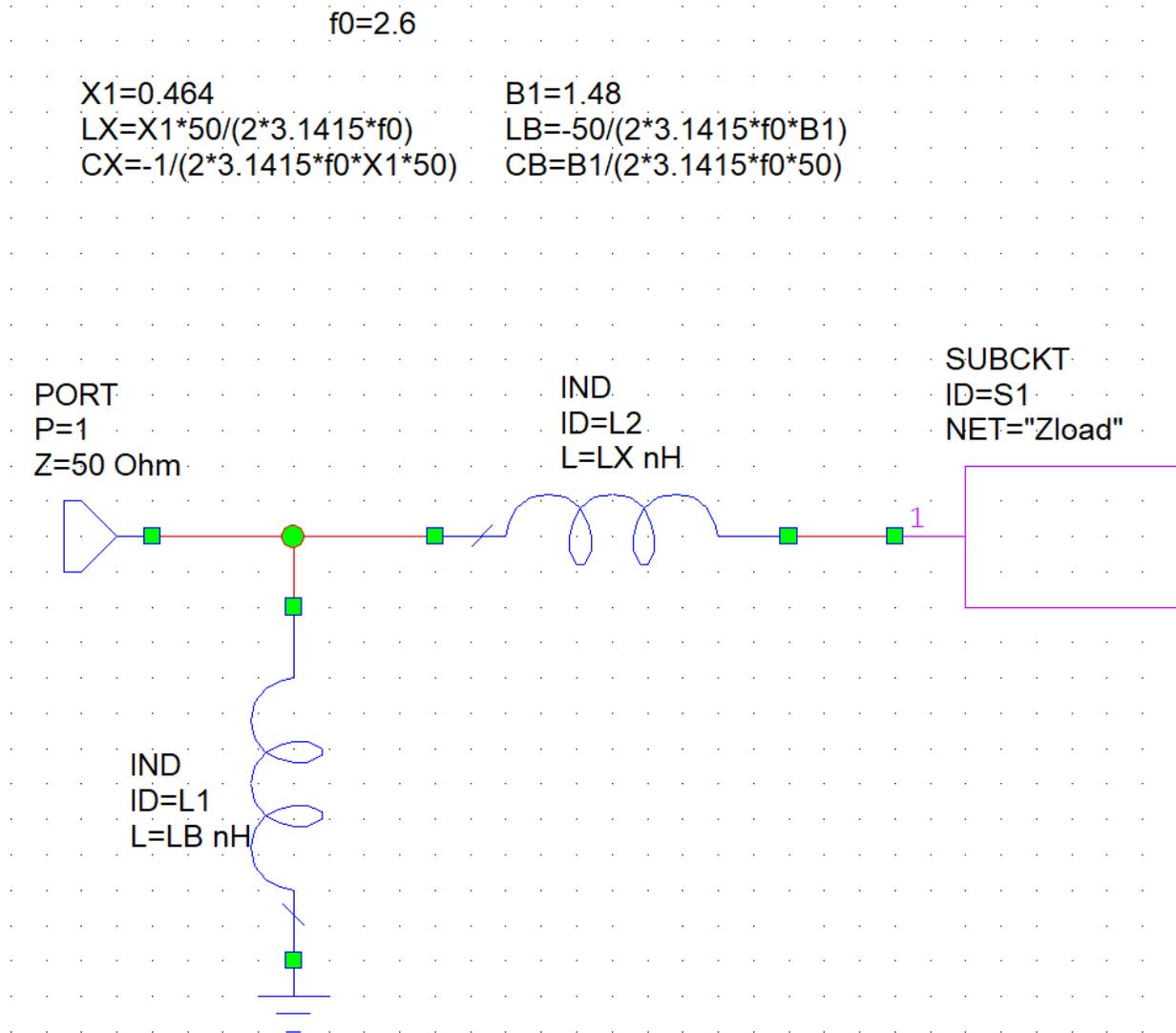


And here are its reflection coefficient characteristics:

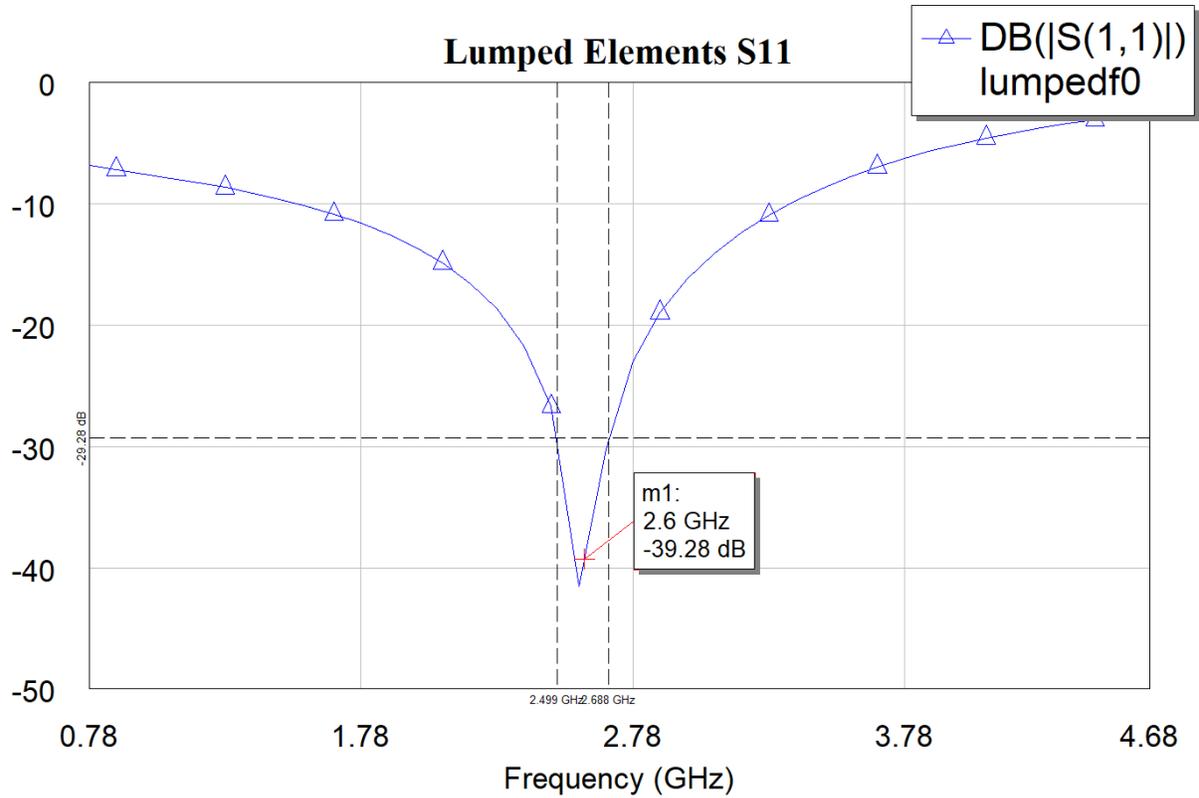


Lumped elements matching circuit:

For this, I chose to use a ladder network to match the load to the port. This is what the circuit looks like:

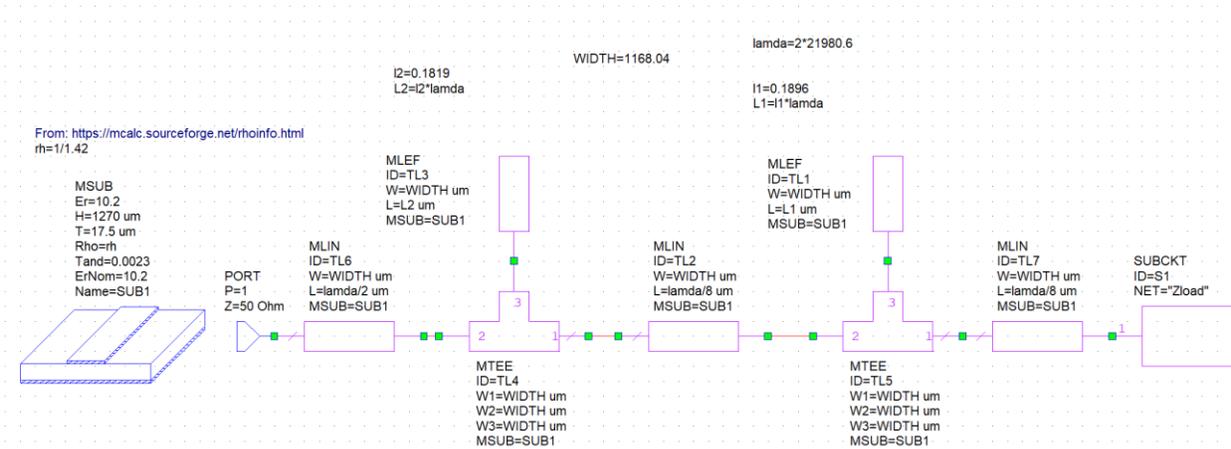


And here are its reflection coefficient characteristics:



Microstrip line double stub matching circuit:

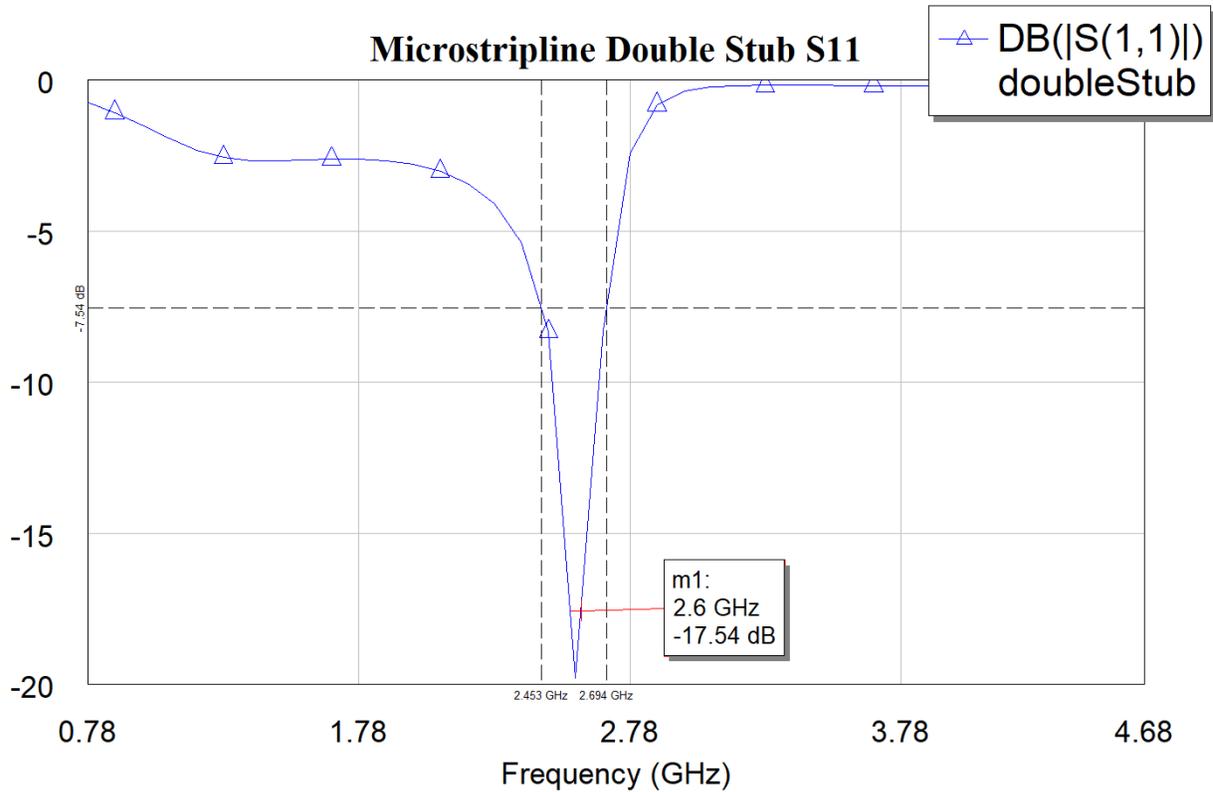
For this design, I first had to add an intermediary transmission line between the first stub and the load to move the load admittance out of the forbidden region of the Smith chart. Also note, the specified substrate was not within the TXLine calculator, so I used the RT/Duroid 5880 preset before replacing the Dielectric Constant and Loss Tangent fields. Therefore, the circuit has the following schematic:



This is the layout:

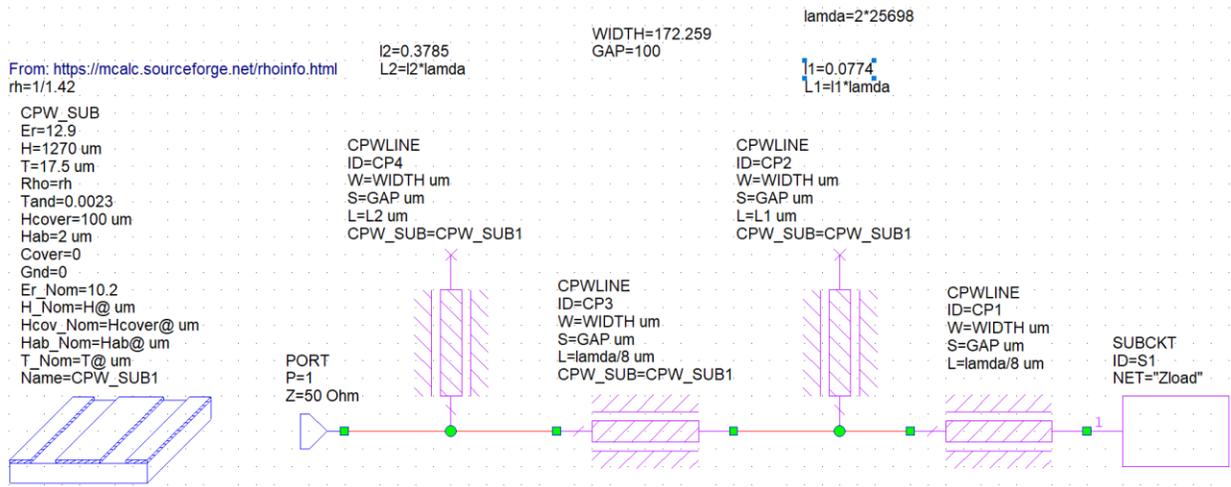


And here are its reflection coefficient characteristics:

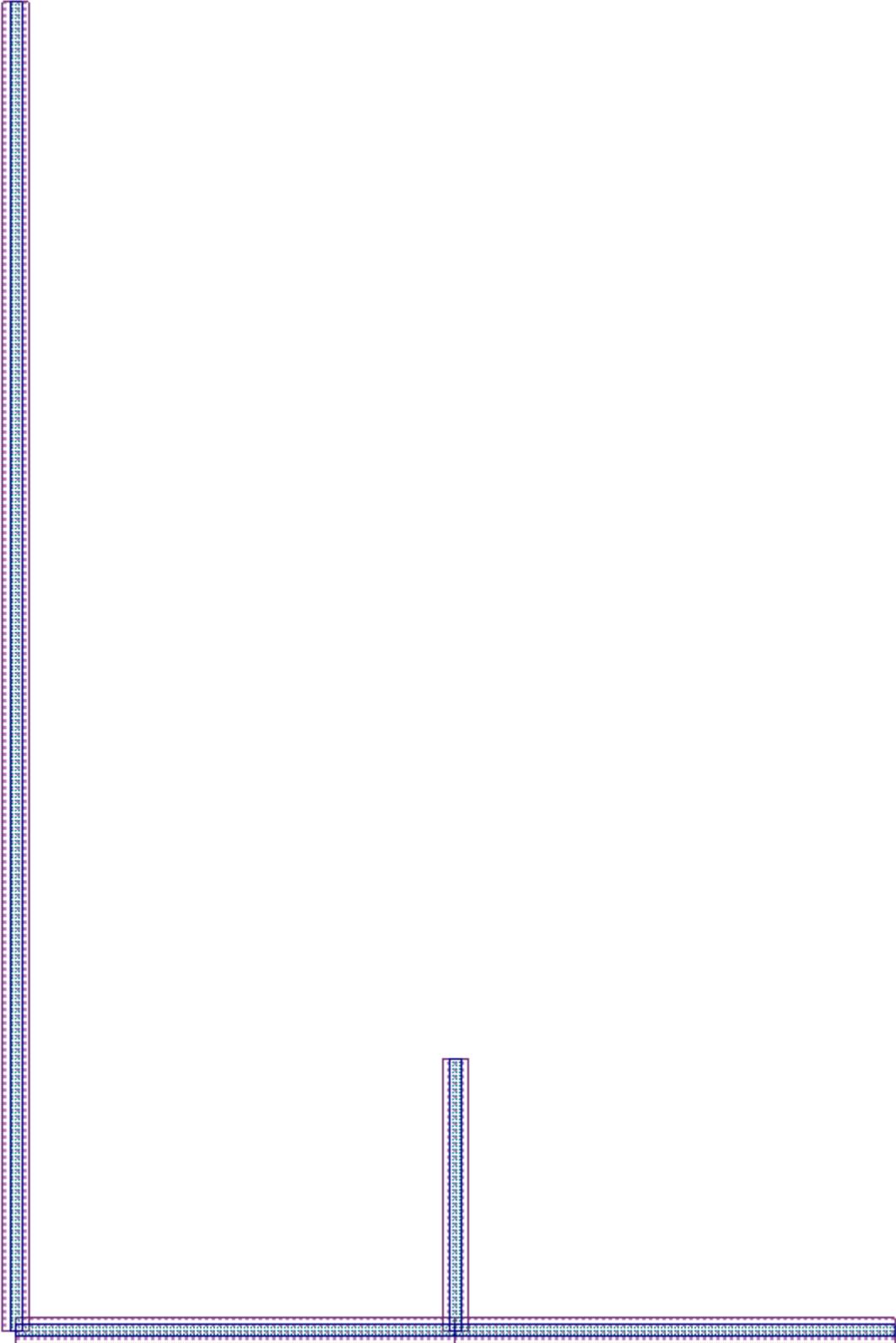


Coplanar waveguide double stub matching circuit:

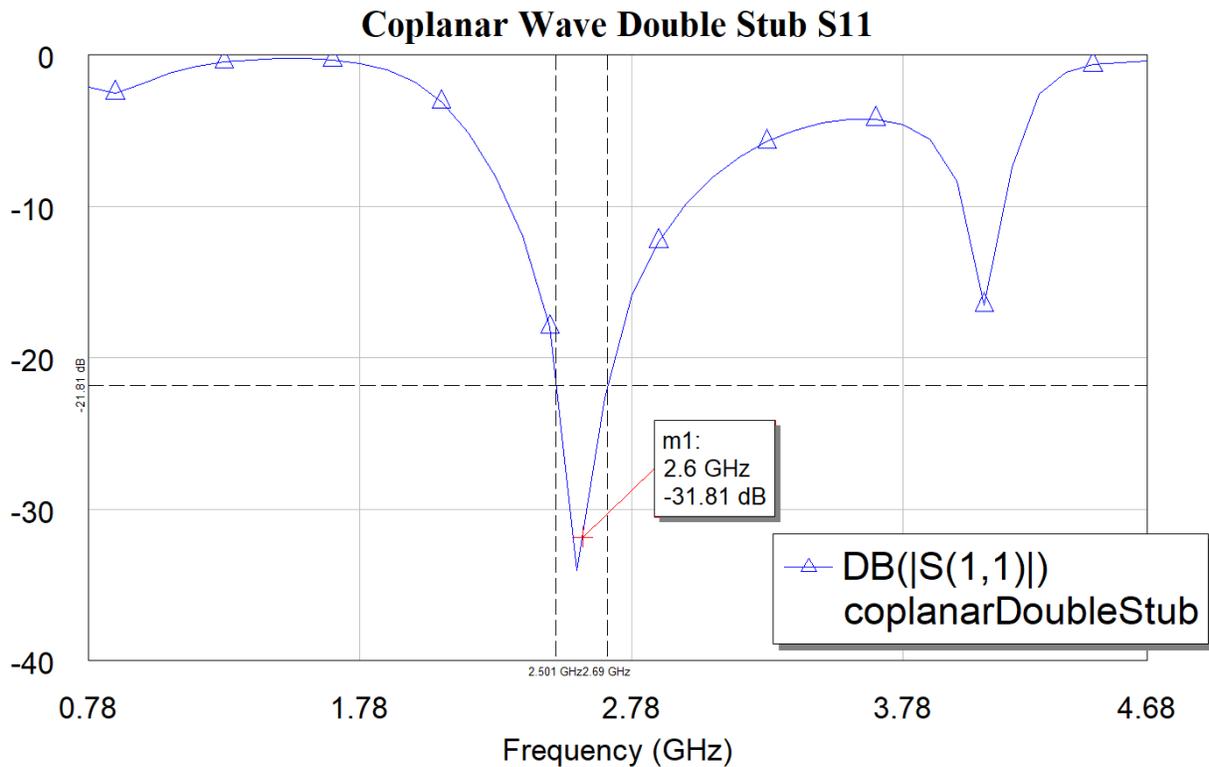
For the coplanar waveguide, I followed the same approach as the microstrip line matching circuit, adjusting the necessary lengths to accommodate for the difference in material parameters. Additionally, T-junctions were not used for this design, and I decided to forego the line towards the port since it is redundant to have a $\frac{\lambda}{2}$ line at that spot. For the gap (“S”) parameter, I chose 100 microns, since the default value of 10 microns produced errors while calculating using the TXLine tool. Here is the schematic:



The layout:



And here are its reflection coefficient characteristics:



Conclusion:

The specific method used to match a load will vastly alter the reflection coefficient, as seen in the above graphs, in both the frequency of interest and far beyond. This means that choosing the appropriate matching network depending on how tight the bandwidth is and sensitive the application is paramount. The quarter-wave transformer had the widest bandwidth and a mediocre reflection coefficient; the microstrip line transformer had a mediocre bandwidth and the highest reflection coefficient; interestingly, the coplanar waveguide transformer and the lumped elements transformer had the same bandwidth, though the lumped elements transformer had a lower reflection coefficient.

It seems that all of my circuits are slightly off the f_0 (or $1.2f_0$) mark, perhaps due to some imprecision in choosing the values for Z_{load} , since all of the designs seem to stray by about the same amount. Some further imprecision can be attributed to choosing the values of the networks' components/lines by using the Smith chart in AWR and tuning the values until they were less than ± 0.01 off the $1 + j0$ mark.

Addendum: Reflection Coefficient Graphs in Terms of Linear Magnitude

In the same order as above:

